IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Richard C. Foss, Peter B. Gillingham, Robert Harland, Masami Mitsuhashi and Atsushi Wada

Application No.: 10/032,431 Group: 2653

Filed: December 21, 2001 Examiner: Dinh, Tan X.

Confirmation No.: 8755

For: DYNAMIC RANDOM ACCESS MEMORY USING IMPERFECT ISOLATING TRANSISTORS

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on 5/27/03 Jennifer A. Tardiff
Date Signature

Jennifer A. Tardiff
Typed or printed name of person signing certificate

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a Reply for filing in the above-identified application.

[ ] Small entity status of this application under 37 C.F.R. 1.9 and 1.27 has been established by a Small Entity Statement previously submitted.

[ ] A Small Entity Statement to establish small entity status under 37 C.F.R. 1.9 and 1.27 is enclosed.

The fee has been calculated as shown below:

	(COL. 1) CLAIMS REMAINING AFTER AMENDMENT		(COL. 2) HIGHEST NO. PREVIOUSLY PAID FOR	(COL. 3) PRESENT EXTRA
TOTAL	8	MINUS	* 20	
INDEP	2	MINUS	** 3	
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

* not fewer than 20
** not fewer than 3

SMALL ENTITY			OR	OTHER THAN SMALL ENTITY	
	RATE	ADDIT. FEE		RATE	ADDIT. FEE
X	$9	$		$18	$
X	$42	$		$84	$
+	$140	$		$280	$
TOTAL =		$ 0		TOTAL =	$ 0

Please charge Deposit Account No. 08-0380 for the following fees:

[ ]	Petition for [ ] month Extension of Time	$
[ ]	Amendment Fee	$
[ ]	Other Fees:	
	_____	$
	_____	$
	TOTAL:	$ 0

A check is enclosed in payment of the following fees:

[X]	Petition for **one** month Extension of Time	$ 110
[ ]	Amendment Fee	$
[X]	Other Fees:	
	Request for Continued Examination	$ 750
	_____	$
	TOTAL:	$ 860

[X] A general authorization is hereby granted to charge Deposit Account No. 08-0380 for any fees required under 37 C.F.R. 1.16 and 1.17 in order to maintain pendency of this application. A copy of this authorization is enclosed for accounting purposes.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
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Concord, Massachusetts 01742-9133
Dated: 5/25/3

::ODMA\MHODMA\iManage;393297;
JM:jat
May 7, 2003

PATENT APPLICATION
Docket No.: 2037.1002-003

Receipt Reissue

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#15

Applicants:	Richard C. Foss, Peter B. Gillingham, Robert Harland, Masami Mitsuhashi and Atsushi Wada	
Application No.:	10/032,431	Group: 2653
Filed:	December 21, 2001	Examiner: Dinh, Tan X.
Confirmation No.:	8755	
For:	DYNAMIC RANDOM ACCESS MEMORY USING IMPERFECT ISOLATING TRANSISTORS	

CERTIFICATE OF MAILING

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on 5/27/03 (Date) Jennifer A. Tardiff (Signature)

Jennifer A. Tardiff
Typed or printed name of person signing certificate

REQUEST FOR CORRECTED FILING RECEIPT

FOR UTILITY APPLICATION

Office of Initial Patent Examination
Customer Service Center
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Technology Center 2600

Sir:

We hereby request that the following items of information be corrected in the Filing Receipt for the subject application received in this office on June 20, 2002.

The Domestic Priority data as claimed by applicant *currently reads*:

THIS APPLICATION IS A REI OF 08/147,038 11/04/93 PAT 5,414,662, WHICH IS A CON OF 07/680,747 04/05/91 ABN.

It should read as follows:

THIS APPLICATION IS A CON OF 08/853,507 05/08/97 PAT RE37,641, WHICH IS A REI OF 08/147,038 11/04/93 PAT 5,414,662, WHICH IS A CON OF 07/680,747 04/05/91 ABN.

Enclosed are copies of the Filing Receipt with changes noted in red and a copy of the first page of specification.

Pursuant to instructions in the February 29, 2000 O.G., we hereby request that the errors which are identified above be corrected in the captioned application to which this request for correction is directed. It is understood that the Patent Office will issue an automatically-generated, corrected Filing Receipt in this and, if applicable, any other affected applications.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

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Date: 1/25/5

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
10/032,431	12/21/2001	2818	1086	2037.1002-003	3	8	2

CONFIRMATION NO. 8755

UPDATED FILING RECEIPT

OC000000008277761

021005
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

OIPE JC124 JUN 0 2 2003 PATENT & TRADEMARK OFFICE

Date Mailed: 06/13/2002

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

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Applicant(s)

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Domestic Priority data as claimed by applicant CON OF 08/853,507 05/08/97 PAT RE37,641, WHICH IS A

THIS APPLICATION IS A REI OF 08/147,038 11/04/1993 PAT 5,414,662
WHICH IS A CON OF 07/680,747 04/05/1991 ABN

Foreign Applications

UNITED KINGDOM 9007789.2 04/06/1990
UNITED KINGDOM 9107164.7 04/05/1991

If Required, Foreign Filing License Granted 03/19/2002

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

RECEIVED
JUN 2 0 2002
HAMILTON, BROOK
SMITH & REYNOLDS, P.C.

Title

Dynamic random access memory using imperfect isolating transistors

Preliminary Class

365

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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YNAMIC RANDOM ACCESS MEMORY USING IMPERFECT ISOLATING TRANSISTORS

This application is a continuation application of Reissue Application Serial No. 08/853,507, filed May 8, 1997, which is based on original U.S. Patent No. 5,414,662; issued May 9, 1995, which was a continuation of Ser. No. 07/680,747, filed Apr. 5, 1991, now abandoned.

FIELD OF THE INVENTION

This invention relates to semiconductor dynamic random access memories (DRAMs) and in particular to apparatus and methods for controlling the sensing of bit lines.

BACKGROUND TO THE INVENTION

A DRAM is generally formed of an array of bit storage capacitors which are accessed via word lines and bit lines, the word lines being located in rows and the bit lines being located in columns. The capacitors are coupled via access transistors to the bit lines upon being enabled by the word lines; each capacitor is thus associated with the intersection of a bit line and word line.

In high speed DRAMs, the bit lines are usually provided as a folded bit line (pairs of complementary bit lines), with a sense amplifier connected to both bit lines of a folded bit line. During a read operation the charge stored on a capacitor is dumped on one of the lines of the folded bit line, and the sense amplifier senses the resulting differential in potential between the two lines of a folded bit line, applying full logic voltage levels to the bit lines which both restore the charge on the storage capacitors and apply full logic levels to data buses to which the bit lines are coupled.

Bit lines typically have a capacitance of around 0.2–0.5 pF. During sensing, current being passed through the sense amplifier to provide full logic voltage levels on the bit lines is consumed in charging the capacitance of the bit lines. The bit line voltage differential must exceed a certain noise margin before the levels on the bit lines can be read to the databuses. Clearly the voltage differential on the lines of the bit lines must be above that certain level, which requires a substantial capacitor charging time, which in turn results in a slowed sensing interval.

A technique for attempting to deal with bit line capacitance is to insert an isolation device to isolate the sense nodes associated with the sense amplifier from the bit lines during the initial sensing period. In other words, a memory capacitor associated with one of the lines of the bit line is enabled to dump its charge on one bit line, following which both bit lines are completely isolated from the sense amplifier. Since the small amount of capacitance associated with the sense node retains some charge differential, subsequent enabling of the sense amplifier causes it to sense this differential, and to apply the full logic level to the sense nodes for application to the databus. Since the sense nodes are now completely isolated from the bit lines, the bit lines need not be charged up by the power supply associated with the sense amplifier, and the time for charging the bit line capacitances thus is substantially eliminated.

However since the capacitance associated with the sense nodes isolated from the bit lines is so small, only a fraction of the total charge differential is available for sensing. This is dangerous, in the sense that the differential can be marginal, and an erroneous bit sensed. In addition, operation of the isolators introduces an additional step in a memory access sequence, sacrificing

It has also been found that the conductive tracks which carry the sense amplifier clock signals must supply considerable current in order to provide, for all sense amplifiers on the chip, full logic levels. That current must not only charge the bit lines and sense nodes, but also the databuses. The conductive tracks across the semiconductor integrated circuit contains resistance, and the heavy clock current passing down the tracks creates a voltage difference. This creates a significant differential in the speed of operation of sense amplifiers close to the sense amplifier clock drivers from those at the far ends of the tracks. Access of data from the memory must be slowed to accommodate the slowest sense amplifier.

SUMMARY OF THE INVENTION

One embodiment of the present invention uses an isolation device as in the prior art described above, but utilizes an imperfect isolation device which can be enabled over an interval and in addition provide a voltage drop. Preferably the isolation device is a field effect transistor (FET) which has its source drain circuit in series between a sense node and an associated bit line. The gate of each FET is held at a voltage which maintains it imperfectly open, and changes to a level which allows each FET to conduct when the sense amplifier operates (e.g. its gate-source voltage is similar to the logic level supplied by the sense amplifier). The imperfect isolation referred to herein means that the source-drain of the FET is in a high resistance state, but allows some charge leakage through it.

Thus when the memory capacitor dumps its charge on the associated bit line, the charge leaks through the imperfect isolation device to the associated sense node of the sense amplifier. During a first part of the sense cycle the voltage on the gate of each isolating field effect transistor is changed to the logic level which is to be applied to the sense amplifier. Due to the leakage through the imperfect isolating device, charge from the memory capacitor leaks to the sense node.

During a subsequent portion of the sense interval, the sense amplifier is enabled. Due to the charge differential between its sense nodes, the sense amplifier applies full logic voltage level to the sense nodes, which is applied to the databuses. However due to the voltage drop across the isolating FET, there is significantly less current consumed in charging the bit line capacitance. As a result the sense nodes reach full logic levels considerably faster than in the prior art.

Some time after sensing is started, the gate source bias of the isolating FET is increased to allow bit lines to be charged to full logic levels (overcoming the threshold voltage drop in the FET). This allows bit line charging current to be distributed over time.

According to an embodiment of the present invention, a dynamic random access memory (DRAM) is comprised of a plurality of bit storage capacitors, a folded bit line for receiving charge stored on one of the capacitors, having bit line capacitance, a sense amplifier having a pair of sense nodes for sensing a voltage differential across the sense nodes, apparatus connected to the bit line and the sense nodes for imperfectly isolating the sense nodes from the bit line whereby current can leak therethrough, apparatus for enabling the sense amplifier and for disabling the isolating apparatus and thereby removing the isolation between the sense amplifier and the bit line, whereby current passing through the sense amplifier to the sense nodes is enabled to